library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity SAU\_EXCLUSIV is

Port (a, b:in bit;

c: out bit);

end SAU\_EXCLUSIV;

architecture Behavioral of SAU\_EXCLUSIV is

begin

c <= a xor b;

end Behavioral;

entity COINCIDENTA is

Port(a, b: in bit;

c: out bit);

end COINCIDENTA;

architecture arh1 of COINCIDENTA is

begin

c <= a xnor b;

end arh1;